EE 505

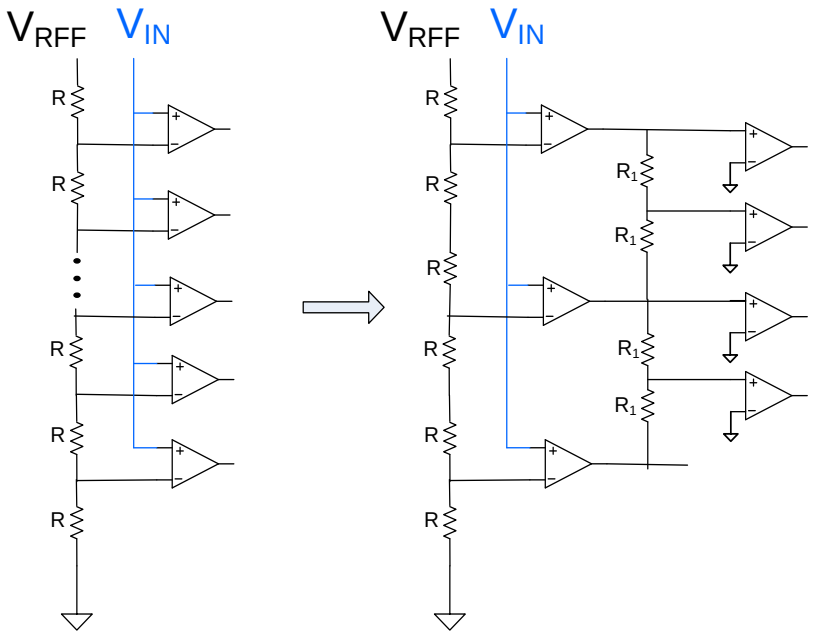
Lecture 22

ADC Design

- Folded
- Multi-Step Flash
- Pipeline

Review from last lecture

Interpolating Flash ADC



Standard Flash

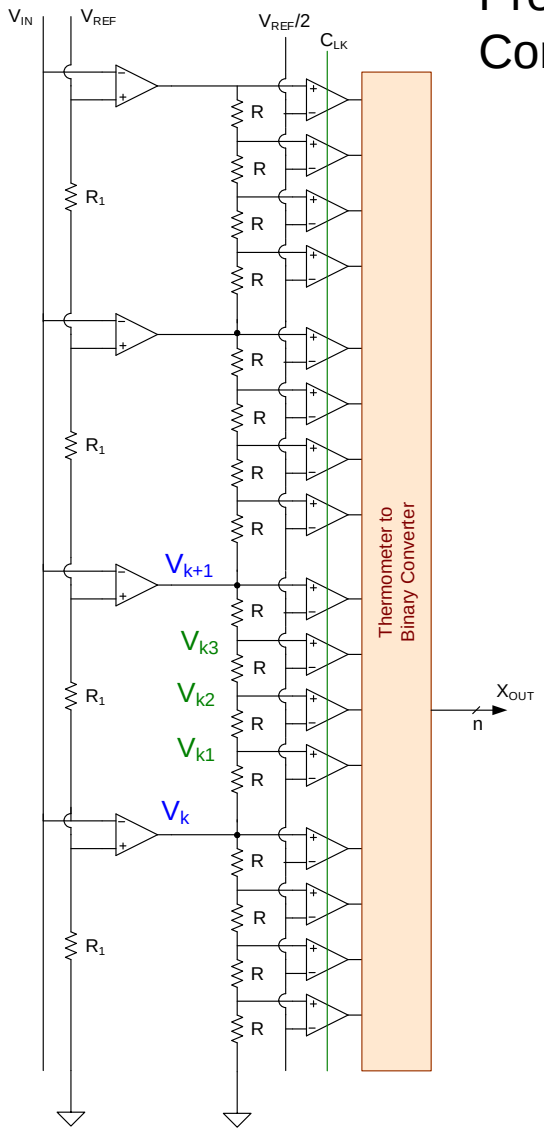
Interpolated Flash

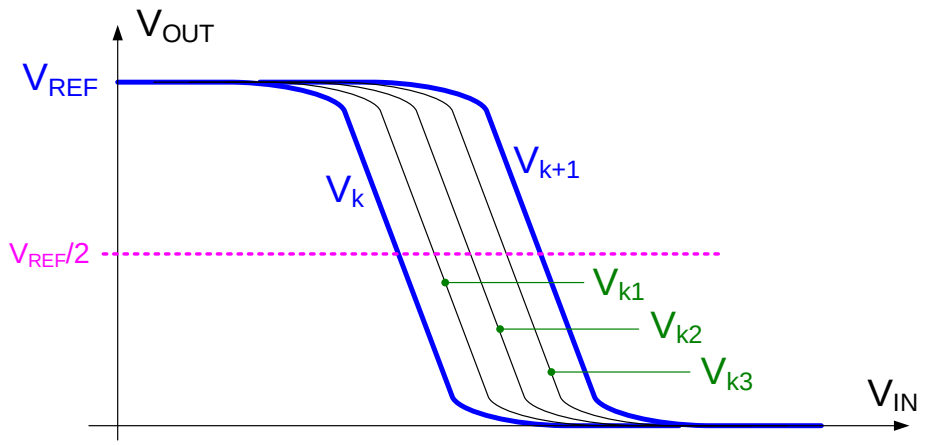
- Reduction in pre-amp area and power
- Latches all referenced to ground
- Loading on V_{IN} reduced
- Kickback to V_{REF} reduced
- V_{IN} coupling to V_{REF} reduced
- Multiple levels can be included in interpolator array

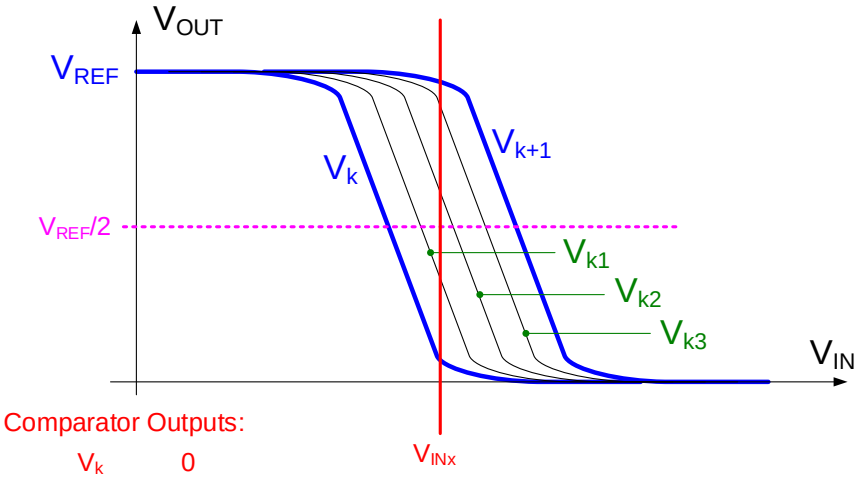
Review from last lecture

Interpolating Flash ADC

4 –levels of interpolation
Preamp gain not critical
Common mode set at $V_{REF}/2$







Comparator Outputs:

V_k	0
V_{k1}	0
V_{k2}	1
V_{k3}	1
V_{k+1}	1

Variants of Interpolating Flash

Patent Number: **5,867,116**

Date of Patent: **Feb. 2, 1999**

Analog Devices

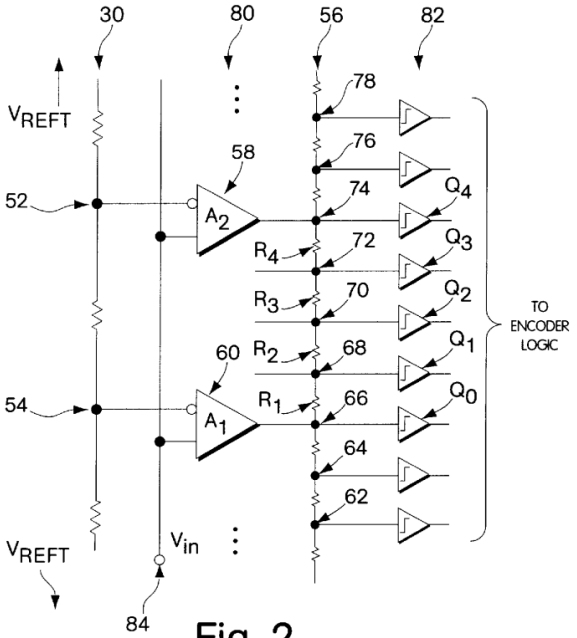


Fig. 2
(PRIOR ART)

Standard R-String Interpolators

Variants of Interpolating Flash

Patent Number: **5,867,116**

Date of Patent: **Feb. 2, 1999**

Analog Devices

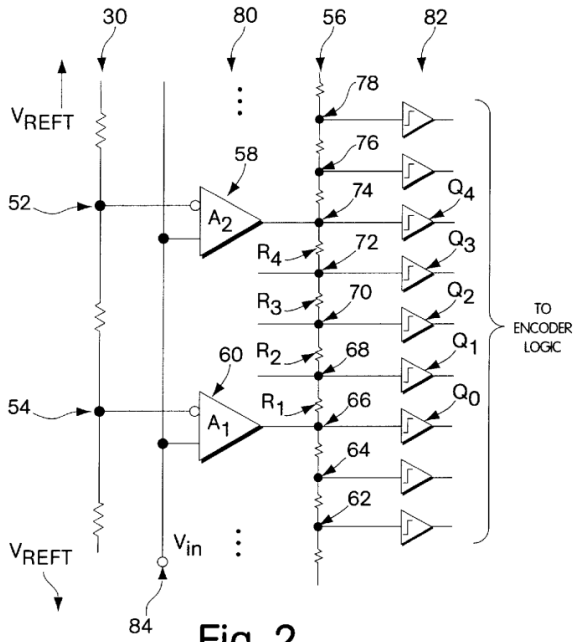
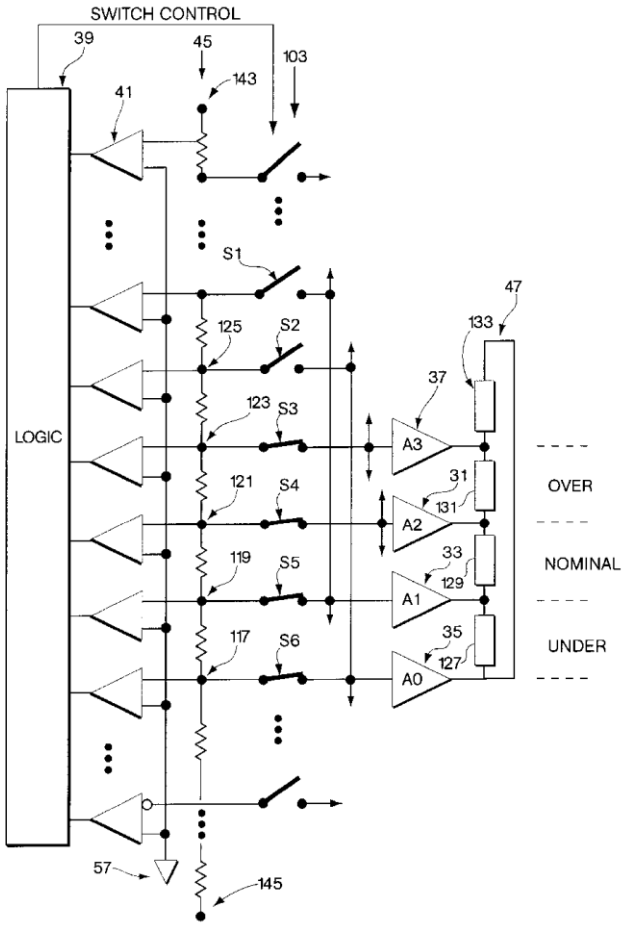


Fig. 2
(PRIOR ART)



Flying Interpolator

Variants of Interpolating Flash

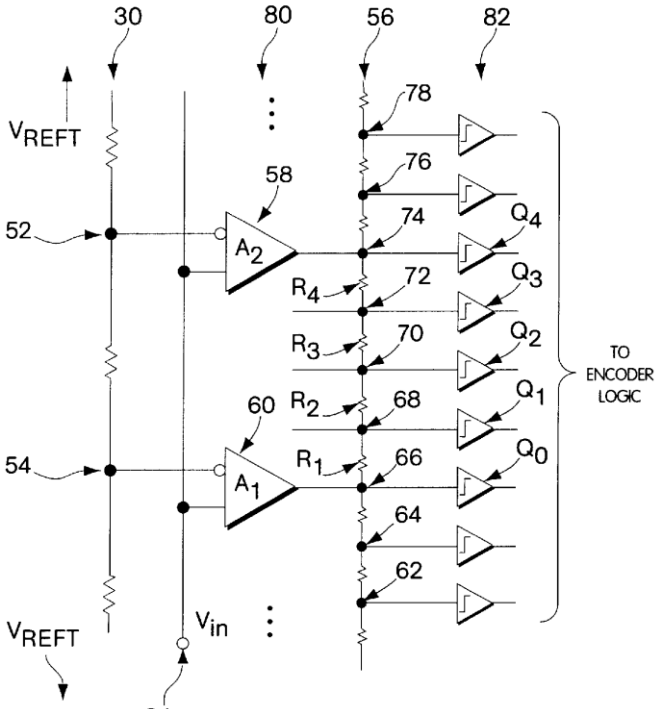


Fig. 2
(PRIOR ART)

Interpolator can be based upon alternative DAC structures

- Current Steering
- Charge Redistribtion

Variants of Interpolating Flash

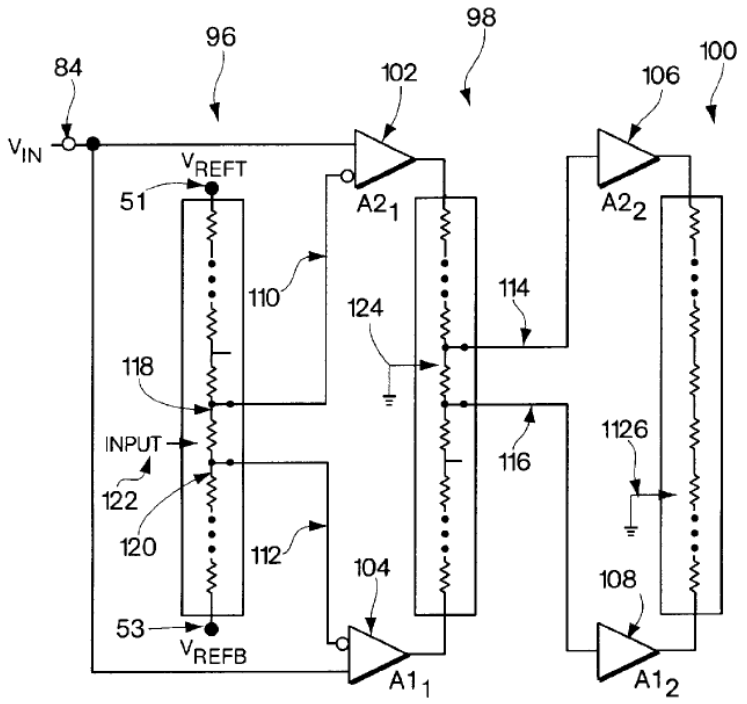


Fig. 11
(PRIOR ART)

Multi-Level Interpolators

Flash ADC Summary

Flash ADC

Very fast

Simple structure

Usually Clocked

Bubble Removal Important

Seldom over 6 or 7 bits of resolution

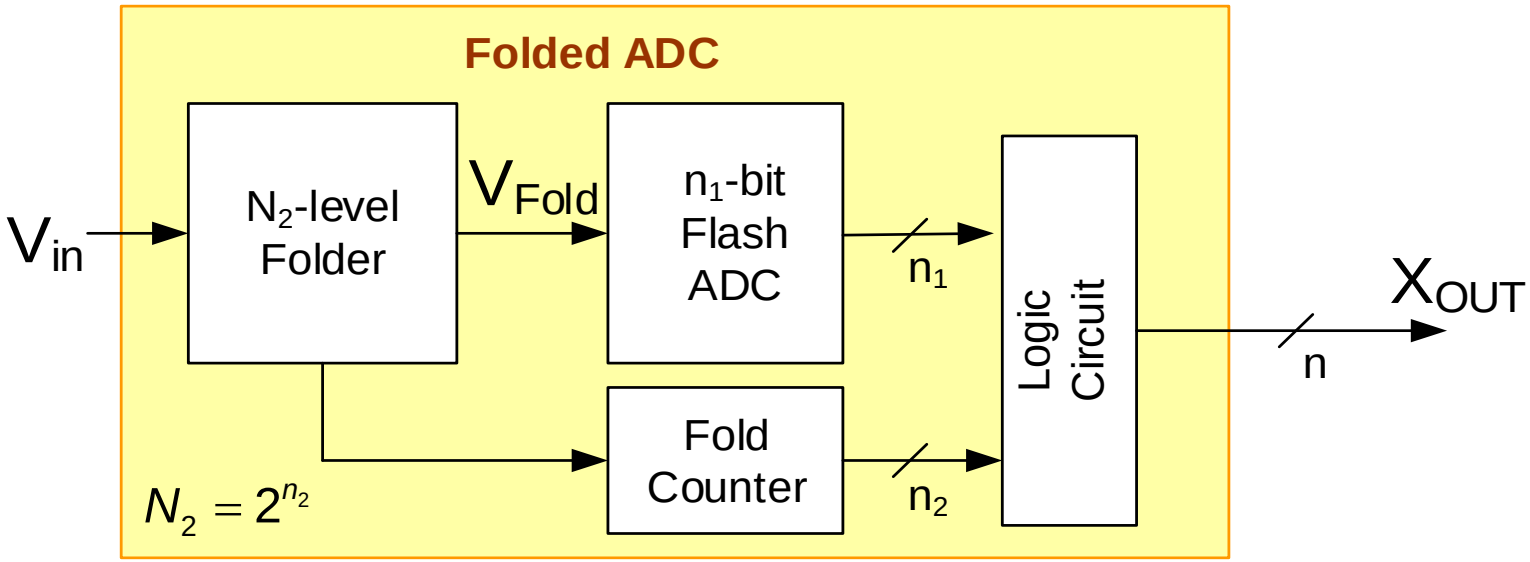
- Flash ADC has some really desirable properties (simple and fast)
- Wouldn't it be nice if we could derive most of the benefits of the FLASH ADC without the major limitations

To be practical at higher resolution, must address the major limitation of the FLASH ADC

Major Limitation of FLASH ADC at higher resolutions?

- **Number of comparators increases geometrically --- 2^n**
- **String DAC area increases geometrically**
- **Too many comparators making non-critical decisions increases power**

Folded ADC Architecture

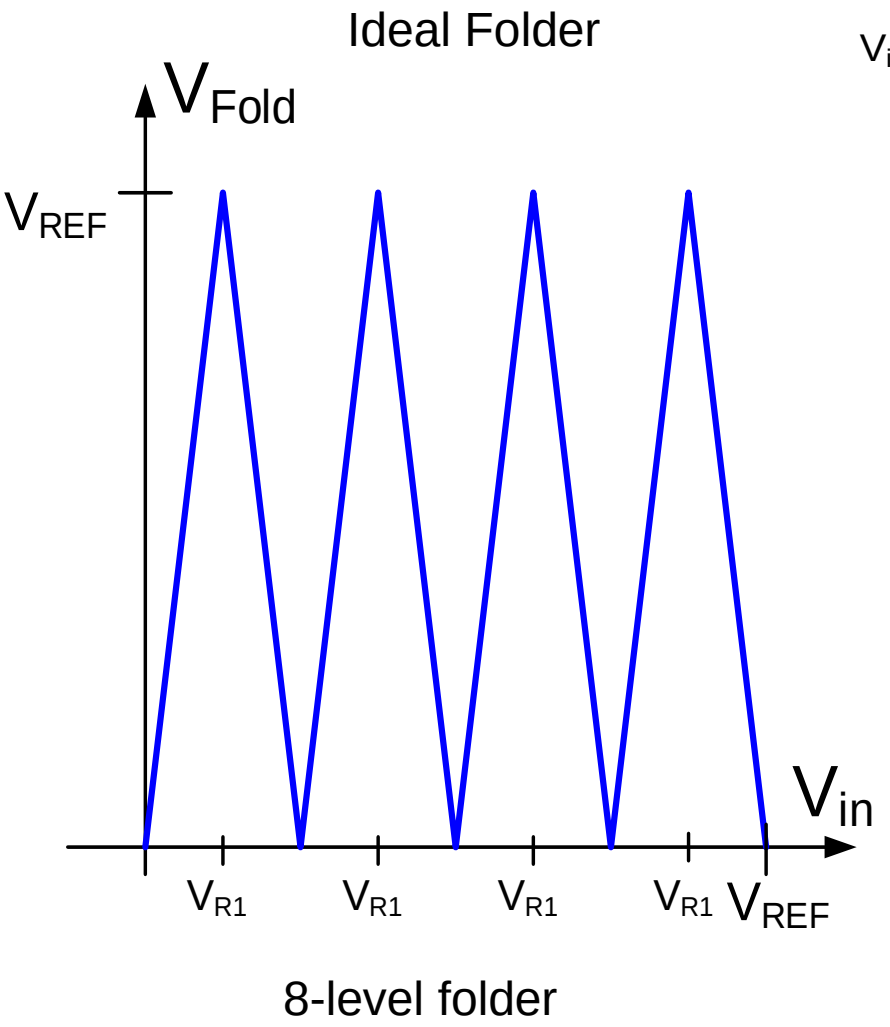


Premise: Folder provides large gain and is very fast

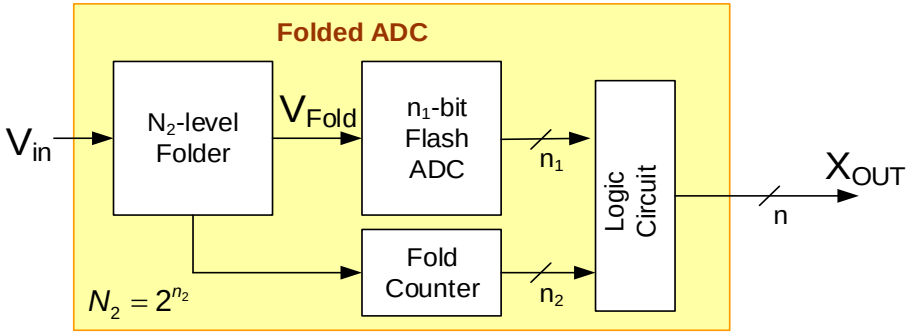
Similar in concept to interpolating flash ADC but

- Number of comparators has been reduced
- Thermometer to Binary decoder is eliminated

Folded ADC Architecture

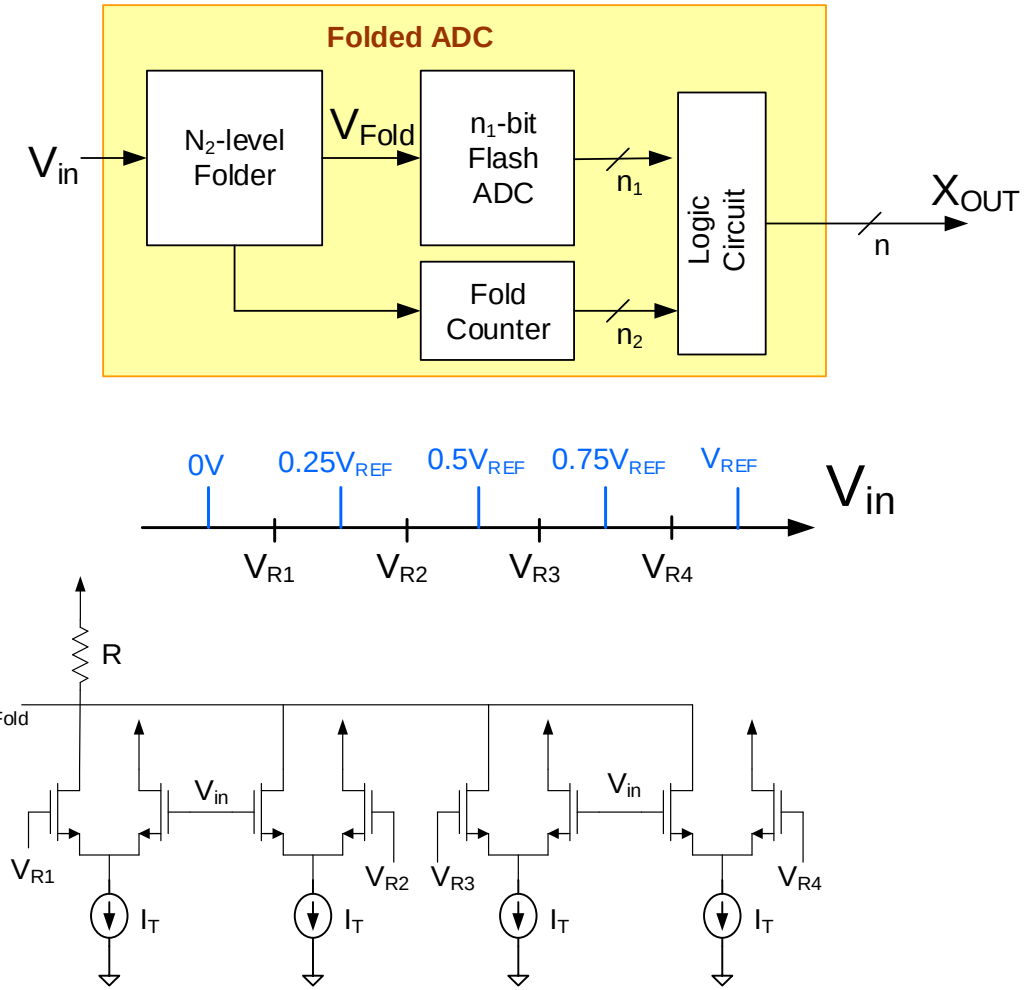


8-level folder



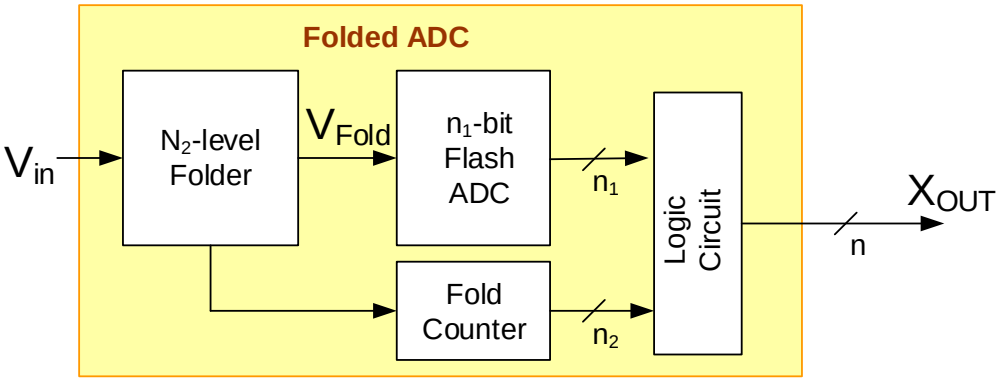
- Provides gain in each fold region
- Effective input range increased from V_{REF} to N_2V_{REF}
- Reduces performance requirements of flash ADC by N_2
- Reduces number of comparators by factor of N_2
- Performance strongly dependent upon performance of folder
- With fast folders, speed comparable to that of a flash ADC
- Architecture of choice by Phillips (now NXP) for high-speed operation for many years (Rudy van de Plassche)
- Competes with pipeline for performance

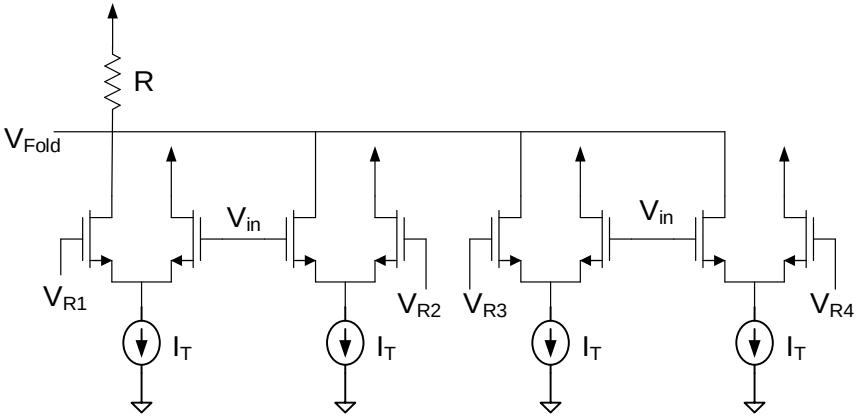
Folded ADC Architecture

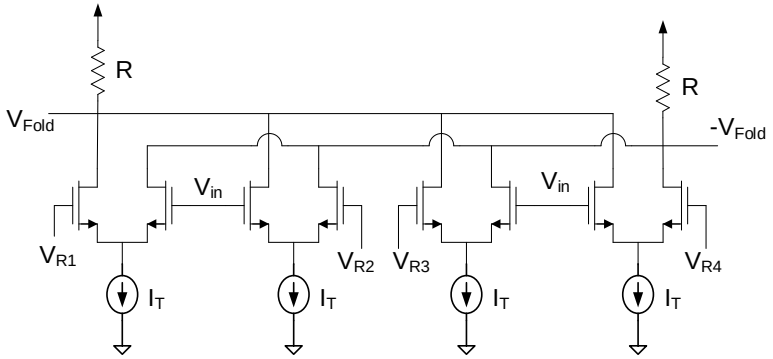


- Requires $N_2/2$ differential amplifiers
- Basic Folder Circuit (8 level)
- Simple Differential Pair can be very fast

Folded ADC Architecture

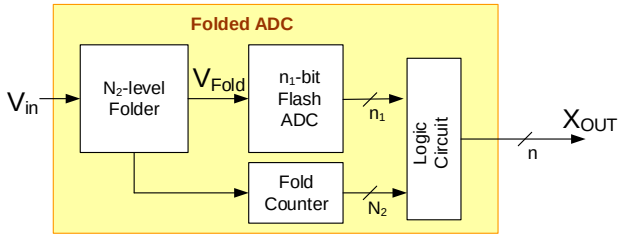




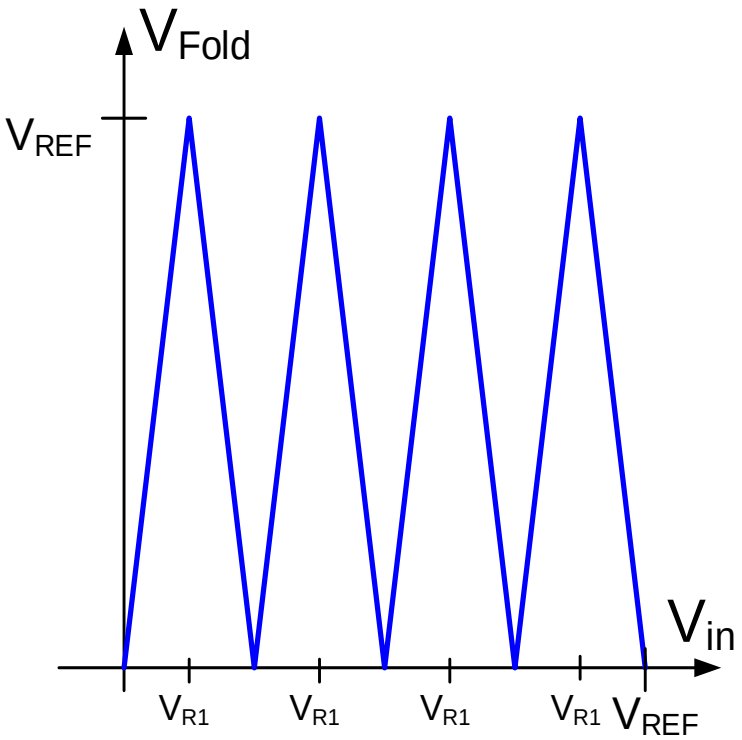


- Usually implemented in differential form
- Differential output almost free

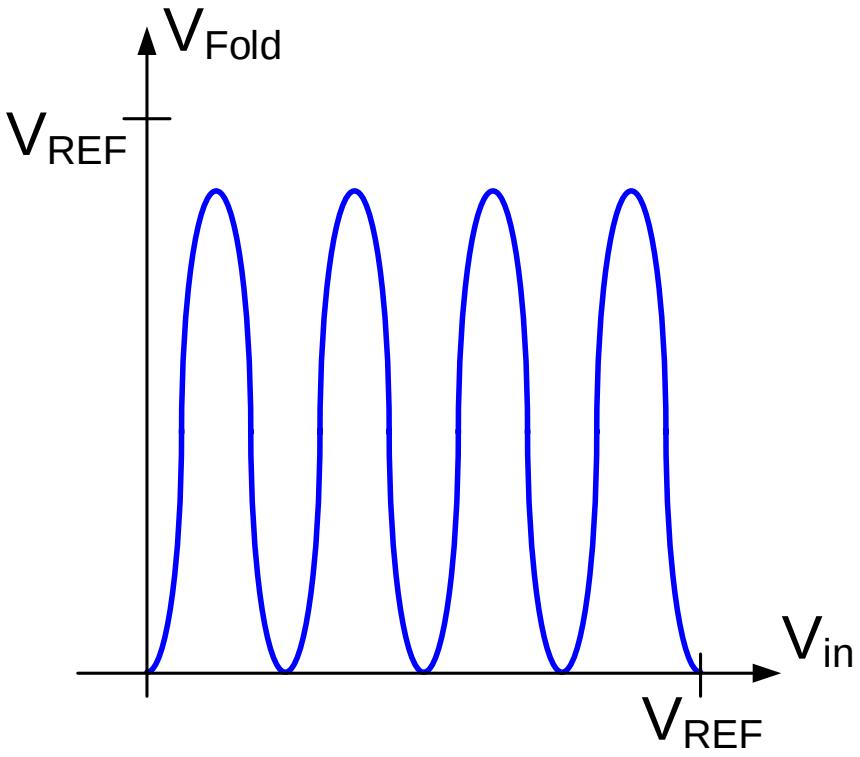
Folded ADC Architecture



Ideal Folder



Typical Folder



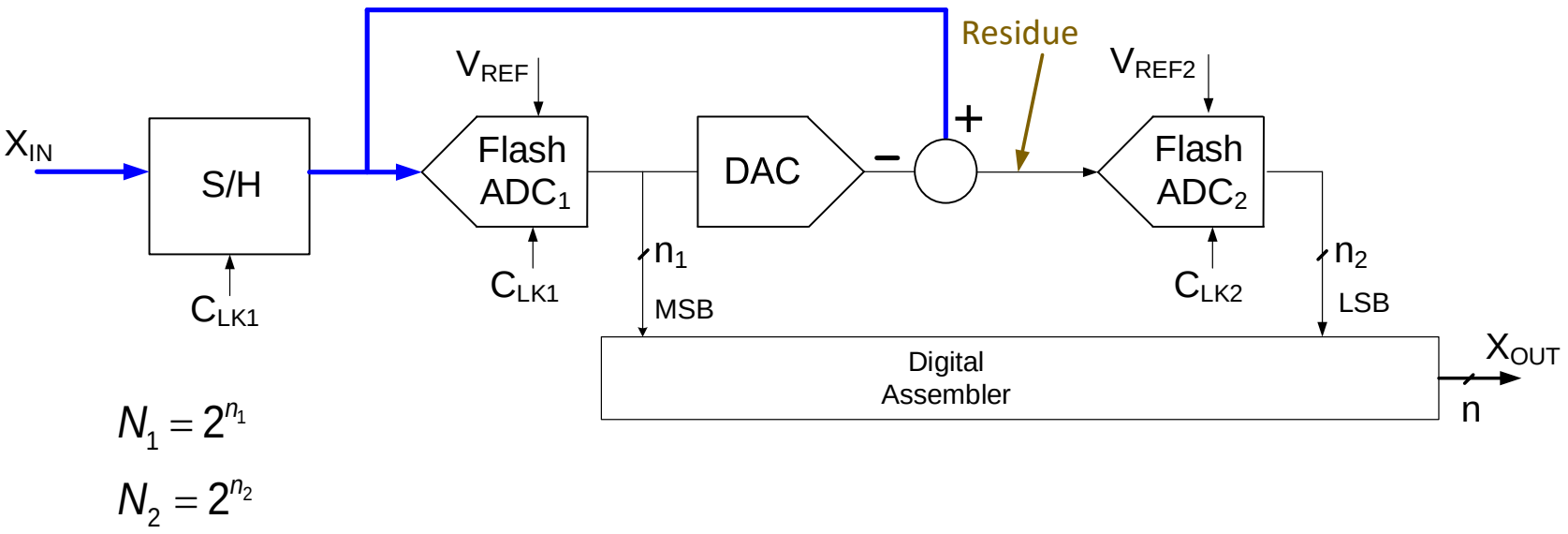
Nonlinearity in folder not a major problem since resolution nonlinearity affects primarily the LSBs and resolution of folded ADCs not large

Multi-Step Flash Approaches

Goal with Multi-Step Flash Approach:

- Reduce number of comparators and sub DAC levels
- Reduce or eliminate un-necessary comparator decisions

Two-Step Flash ADC



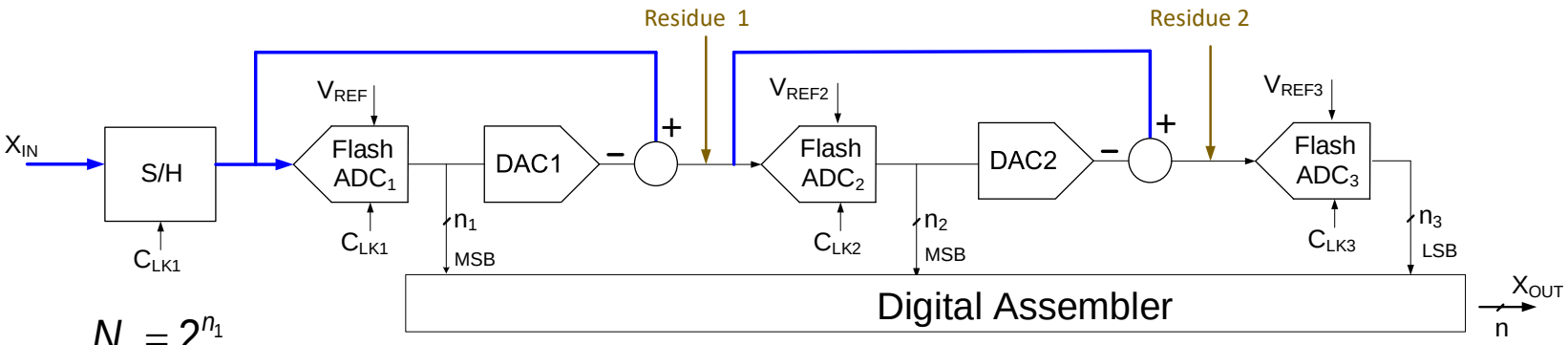
$N_1 = 2^{n_1}$

$N_2 = 2^{n_2}$

- Can operate asynchronously after S/H
- If clocked, C_{LK2} must be delayed from C_{LK1}
- Full-range of Residue signal is V_{REF}/N_1
- Reduces number of comparators from $2^{n_1+n_2}$ *to* $2^{n_1} + 2^{n_2}$
- V_{REF2} can be reduced by a factor of N_1 from V_{REF}

- No improvement in offset requirements on comparators of second-stage flash
- Common-mode signal swing on comparators in second-stage flash reduced by factor of N_1
- DAC accuracy and difference amplifier performance important

Three-Step Flash ADC



$$N_1 = 2^{n_1}$$

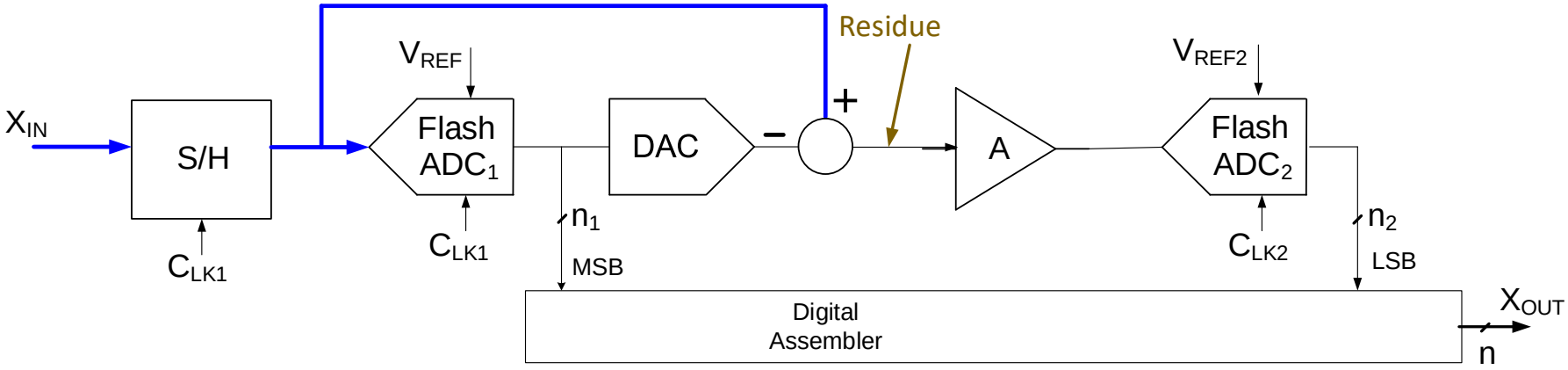
$$N_2 = 2^{n_2}$$

$$N_3 = 2^{n_3}$$

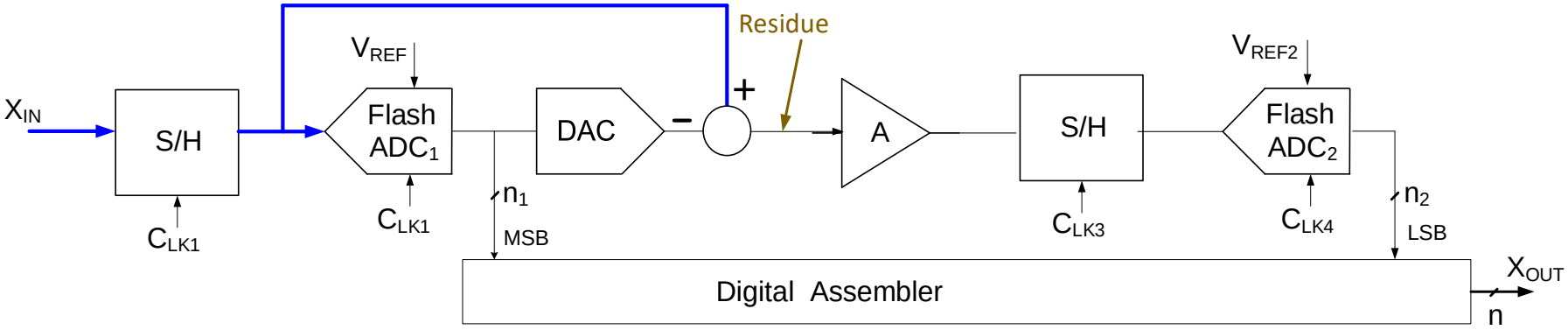
- Can operate asynchronously after S/H
- Full-range of Residue 2 signal is $V_{REF}/(N_1N_2)$
- Reduces number of comparators by factor from $2^{n_1+n_2+n_3}$ *to* $2^{n_1}+2^{n_2}+2^{n_3}$
- V_{REF3} can be reduced by a factor of N_2 from V_{REF2}

- No improvement in offset requirements on comparators of second-stage flash
- Common-mode signal swing on comparators in second-stage flash reduced by factor of N_1
- DAC accuracy and difference amplifier performance important

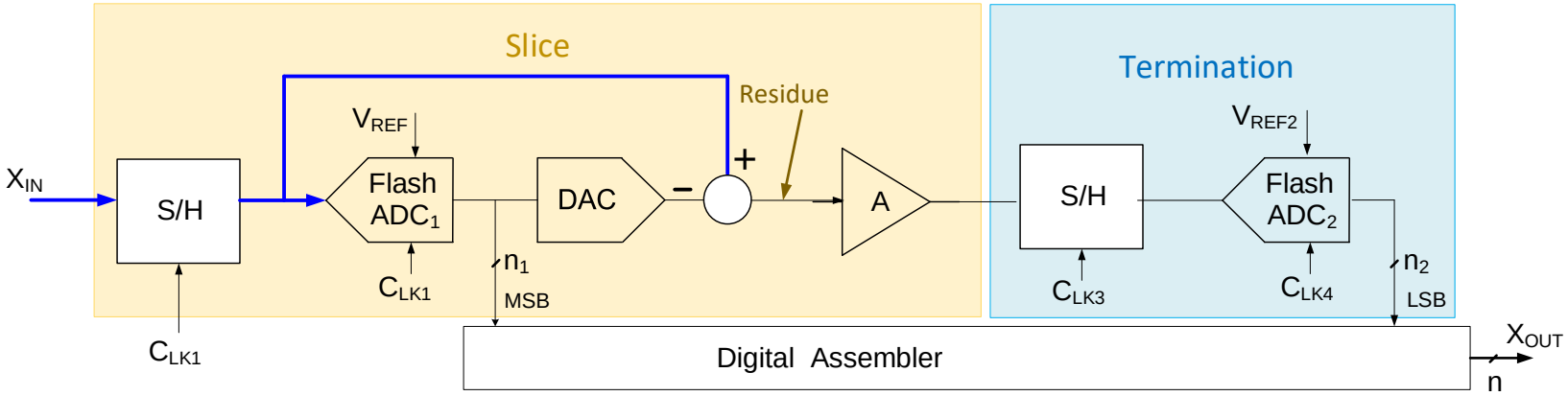
Two-Step Flash ADC with Interstage Gain



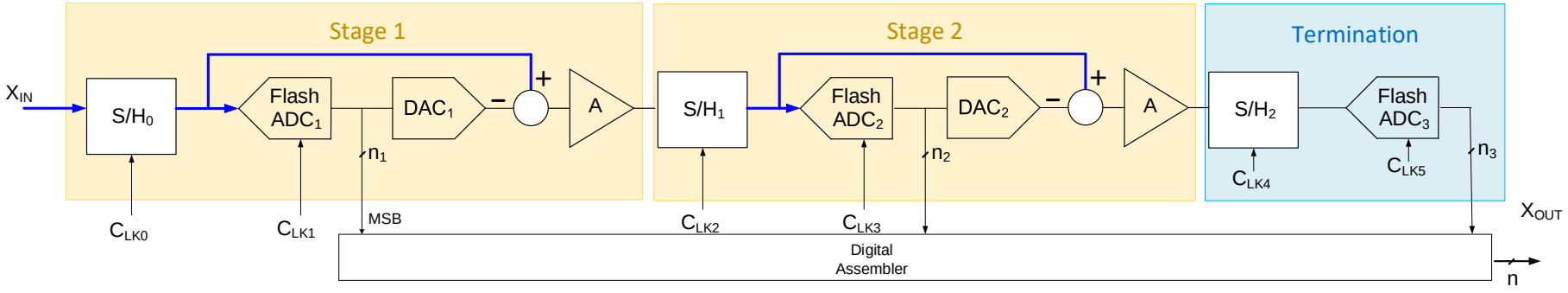
Two-Step Flash ADC with Interstage Gain and S/H



Slice which could be repeated

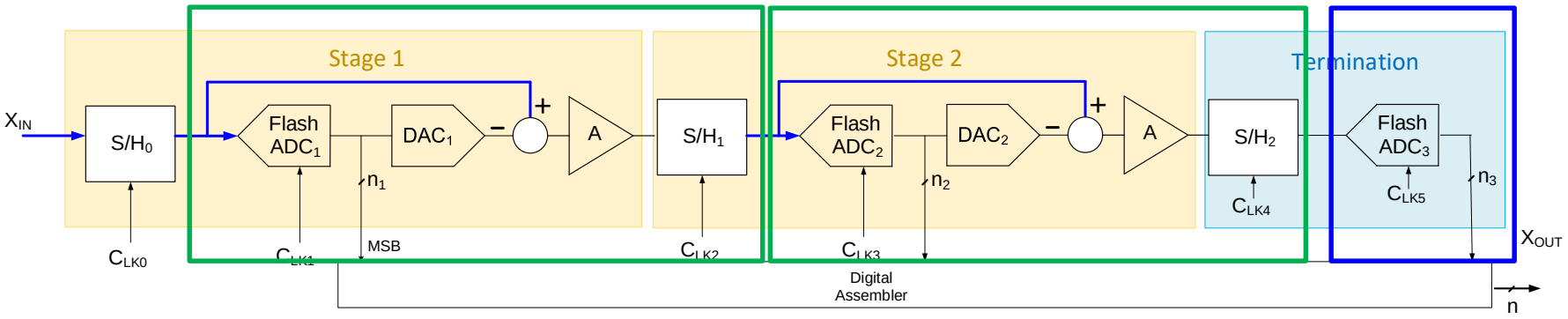


Three-Step Flash ADC with Interstage Gain and S/H



- S/H frees first stage to take another sample during second stage conversion
- This has a pipelining capability
- The pipelined approach dramatically improves speed (close to Flash)
- Significantly reduces the number of comparators
- Introduces latency but not of concern in most applications

Three-Step Flash ADC with Interstage Gain

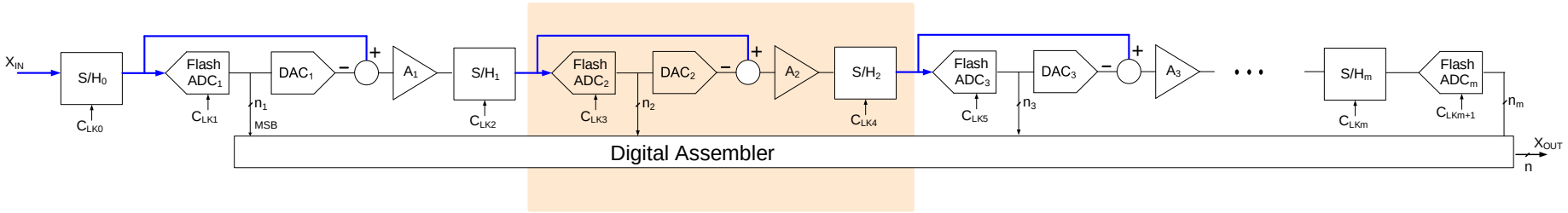


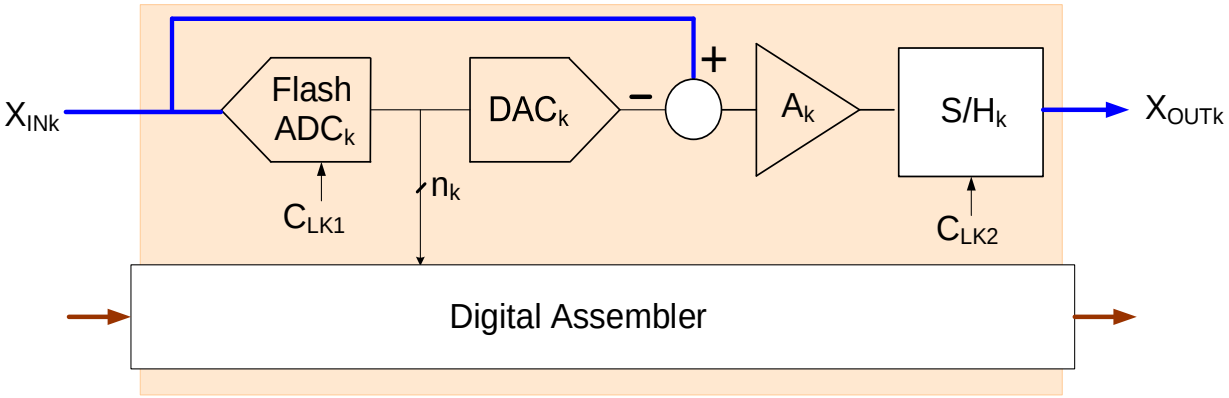
Can be extended to more than 3 stages

- Can go up to 16 bits or maybe a little higher
- Could be as few as one comparator in each Flash ADC
- Further reduction in number of comparators
  (e.g. if one comparator per stage, need only n comparators)
- More latency with more stages but still seldom of concern
- If gains are large enough, comparator offsets in later states can be large
- Will show that with minor modifications, comparator offsets can even be large in first stage

Can partition stages differently

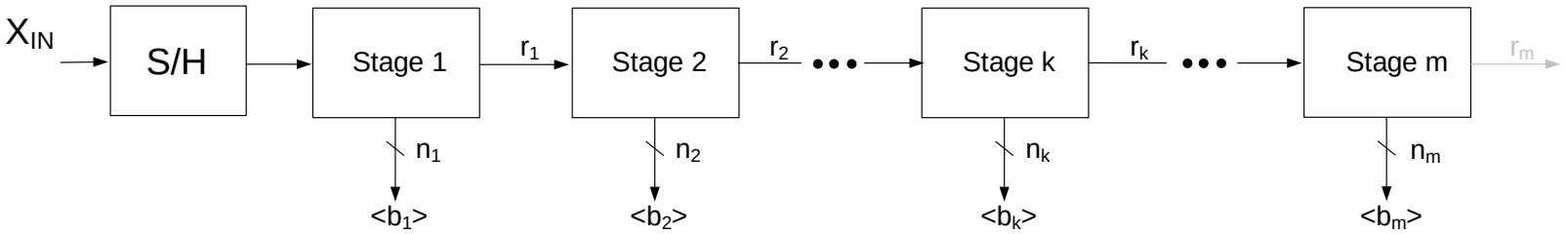
Pipelined ADC





Pipeline Stage

Pipelined ADC



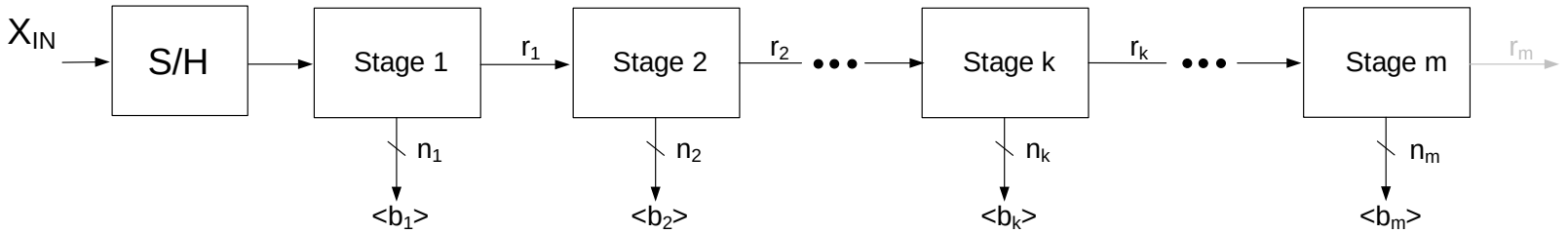
Digital Assembler can simply concatenate individual outputs for some stage architectures

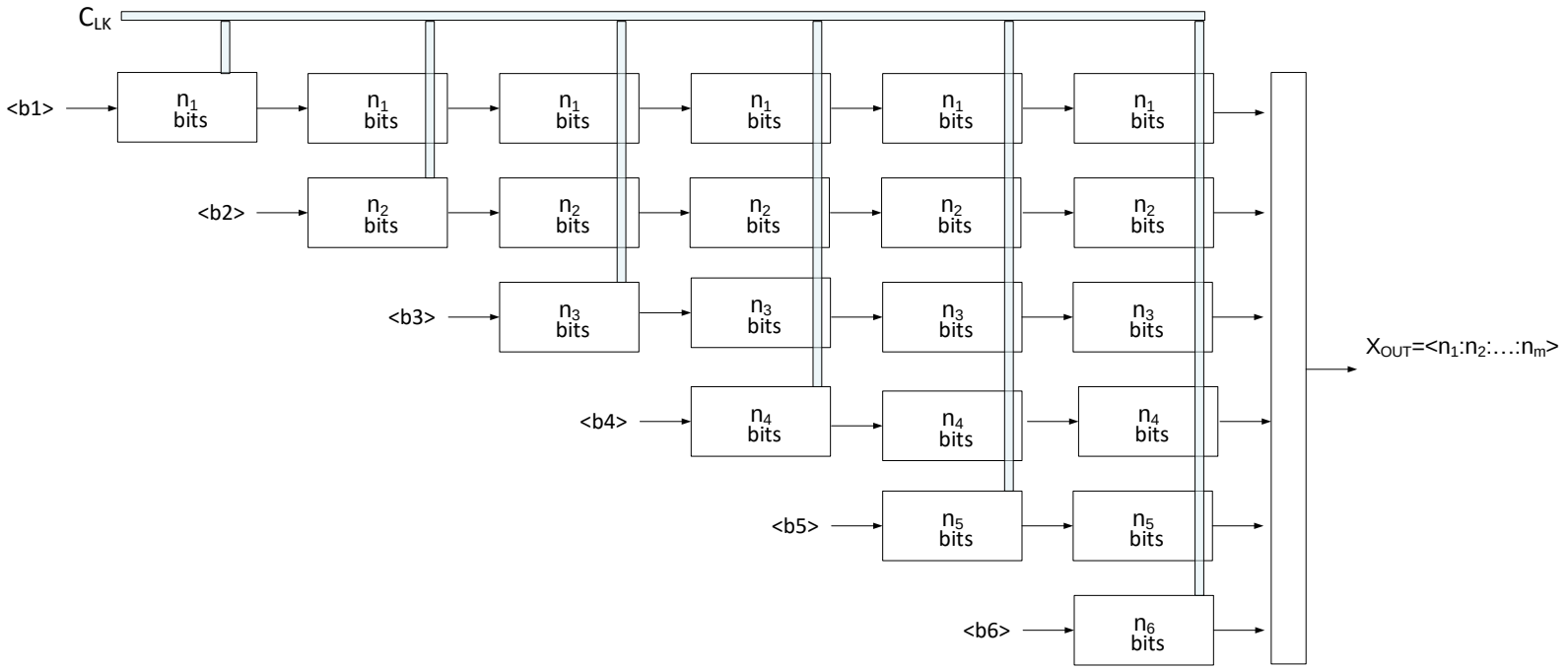
$$X_{OUT}=<n_1:n_2:\ldots:n_m>$$

In this case the Digital Assembler can be a set of m-parallel shift-register blocks with output on the last stage

Latency is equal to the number of stages times the conversion time/stage

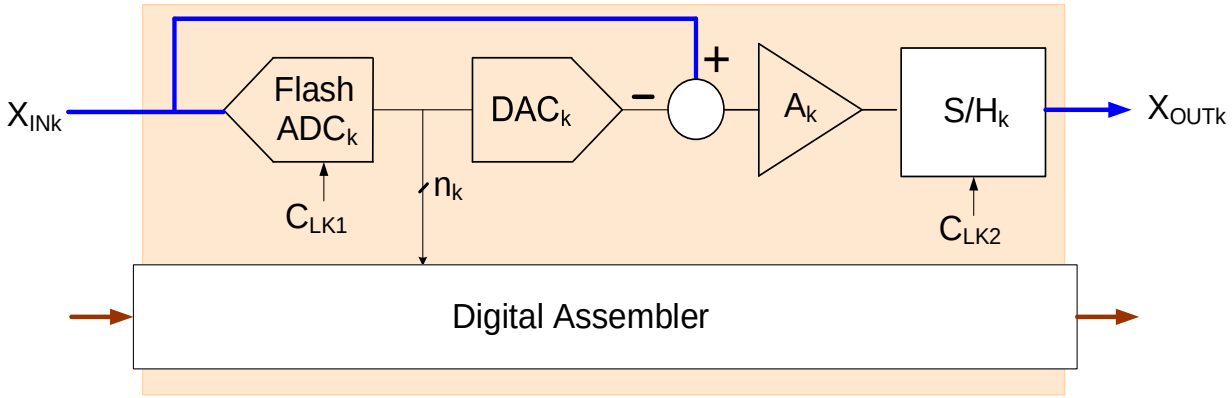
Pipelined ADC





Digital Assembler

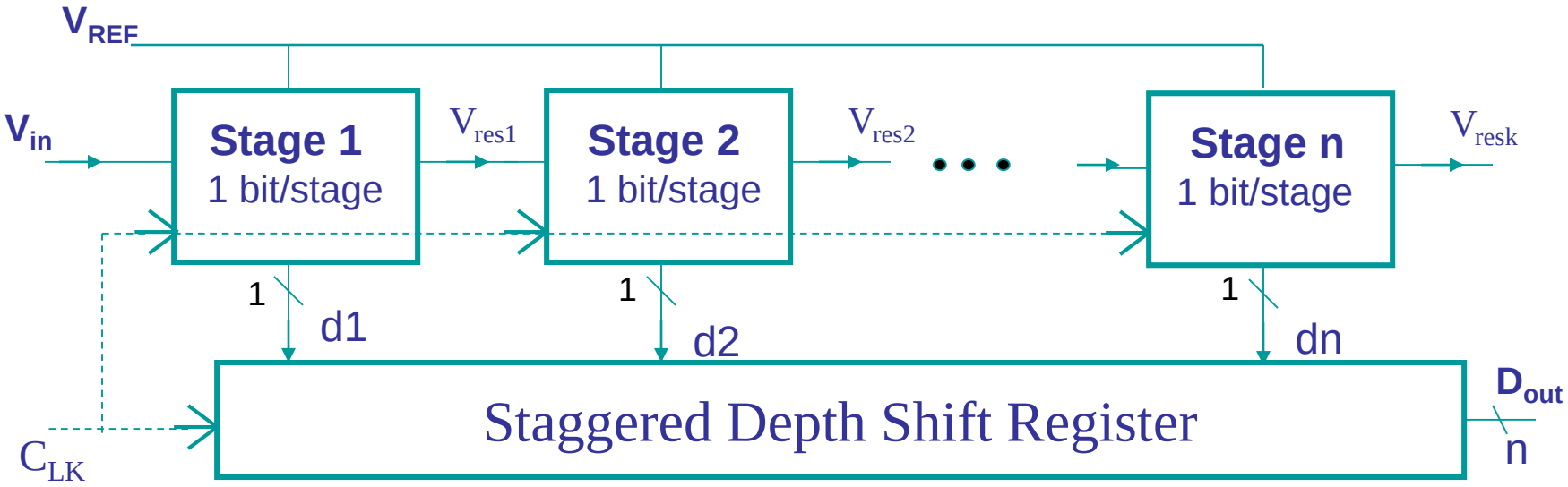
Pipeline Stage



- Appears to be lots of complexity
- S/H is sampling a near-static signal on all stages (except stage 0)
- Ideally the stage gain is chosen so for maximum signal level at the output is V_{REF} for each stage
- Dominant source of power dissipation is typically the amplifier

Example of 1 bit/stage pipeline

- A=2
- ADC is simply comparator in each stage
- Stages could be identical though often relaxed requirements on latter stages to reduce power

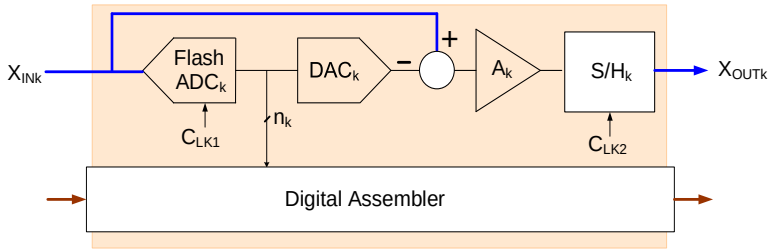


D_{OUT} = <d1 d2 … dn>

$$V_{OUT} = V_{REF} \sum_{i=1}^{n} \frac{d_i}{2^i}$$

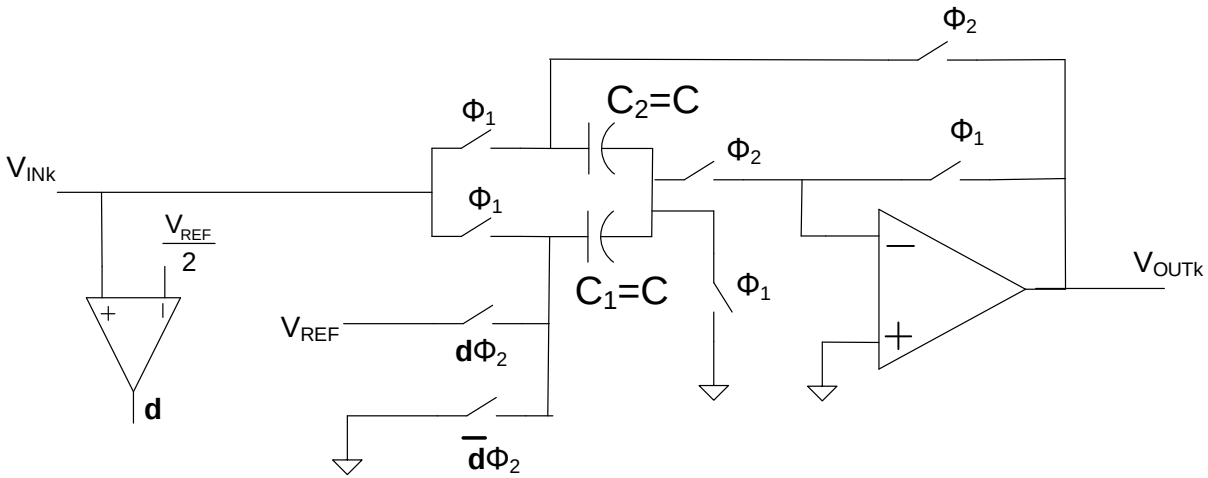
- Functional form of output particularly attractive and simple
- Similar relationship for any integral number of bits/stage

Typical SC Pipeline Stage

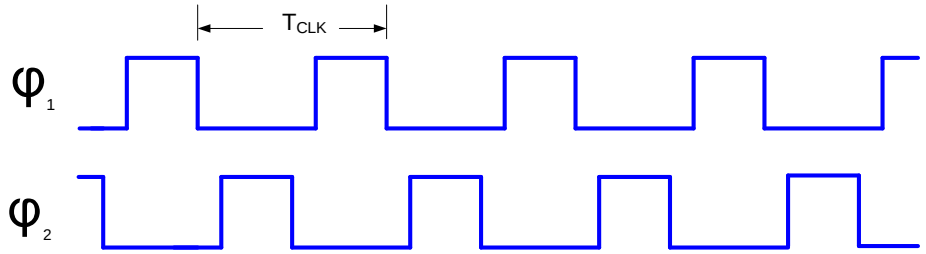


Very simple and compact stages are used

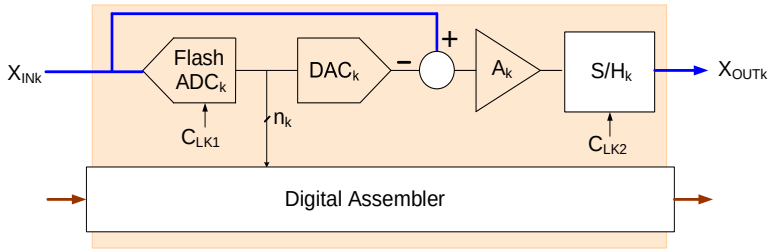
For 1 bit/stage (Digital Assembler not shown)



Clock is complimentary nonoverlapping

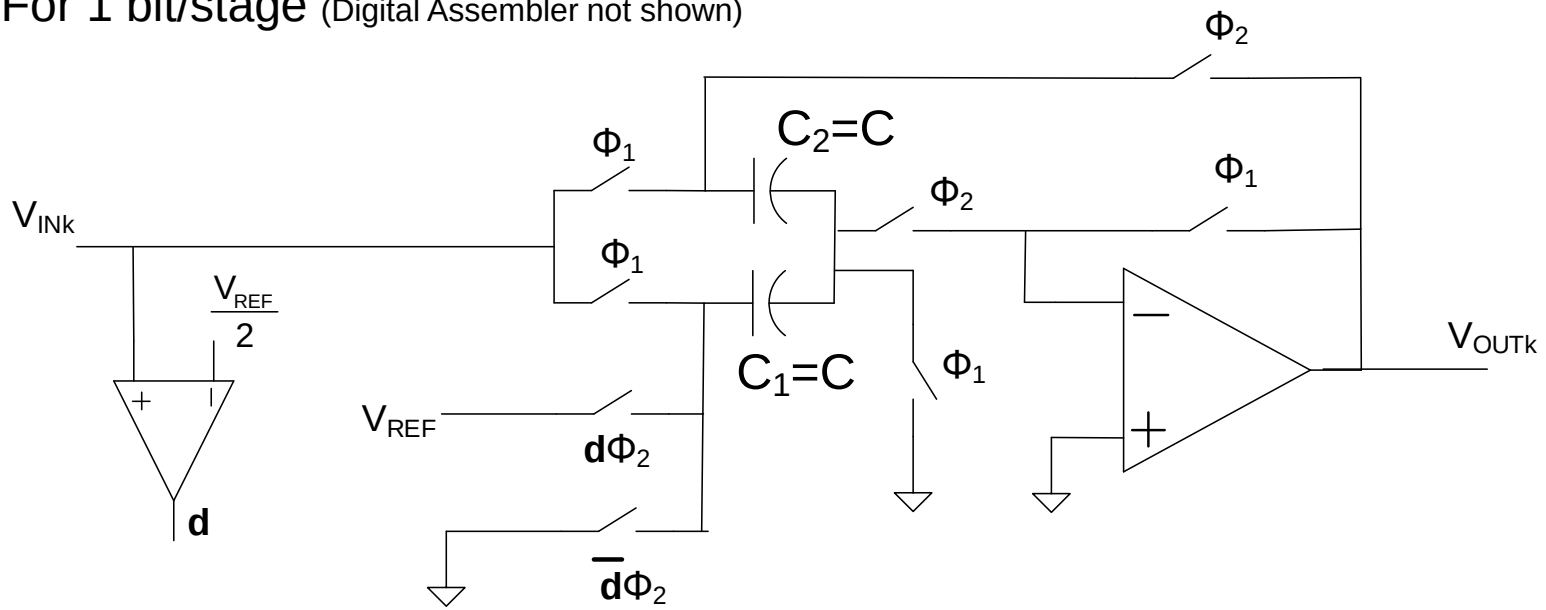


Typical SC Pipeline Stage



Very simple and compact stages are used

For 1 bit/stage (Digital Assembler not shown)



Gain =2

$$V_{OUT}=V_{IN}\left(1+\frac{C_1}{C_2}\right)-d\left(\frac{C_1}{C_2}\right)V_{REF} \quad \Rightarrow \quad V_{OUTk}=2V_{INk}-dV_{REF}$$

End of Lecture 22